UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,018	01/03/2001	Motoshi Ito	YAMAP0748US	3434

7590 09/20/2005	**EXAMINER**
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Renner, Otto, Boisselle, & Sklar, L.L.P.	
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ART UNIT	PAPER NUMBER
2131	

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DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/754,018	ITO ET AL.
	Examiner	Art Unit
	Matthew T. Henning	2131

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>*29 June 2005*</u>.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-3 and 5-9* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) *1-3 and 5-9* is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on <u>*03 January 2001*</u> is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☒ All b) ☐ Some * c) ☐ None of:
        1. ☒ Certified copies of the priority documents have been received.
        2. ☐ Certified copies of the priority documents have been received in Application No. _____.
        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1   This action is in response to the communication filed on 6/29/2005.

2   **DETAILED ACTION**

3   *Continued Examination Under 37 CFR 1.114*

4   A request for continued examination under 37 CFR 1.114, including the fee set forth in

5   37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

6   eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

7   has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

8   37 CFR 1.114. Applicant's submission filed on 6/29/2005 has been entered.

9   *Response to Arguments*

10   Applicant's arguments with respect to claims 1-3, and 5-9 have been considered but are

11   moot in view of the new ground(s) of rejection.

12   Claims 1-3, and 5-9 have been examined. Claim 4 has been cancelled.

13   All objections and rejections not specifically set forth below have been withdrawn.

14   *Drawings*

15   The drawings are objected to under 37 CFR 1.83(a). The drawings must show every

16   feature of the invention specified in the claims. Therefore, the data scramble circuit acting as

17   part of an error correction circuit must be shown or the feature(s) canceled from the claim(s). No

18   new matter should be entered.

19   Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to

20   the Office action to avoid abandonment of the application. Any amended replacement drawing

21   sheet should include all of the figures appearing on the immediate prior version of the sheet,

22   even if only one figure is being amended. The figure or figure number of an amended drawing

1   should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

2   must be removed from the replacement sheet, and where necessary, the remaining figures must

3   be renumbered and appropriate changes made to the brief description of the several views of the

4   drawings for consistency. Additional replacement sheets may be necessary to show the

5   renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

6   application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

7   pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

8   be notified and informed of any required corrective action in the next Office action. The

9   objection to the drawings will not be held in abeyance.

10   *Claim Rejections - 35 USC § 103*

11   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

12   obviousness rejections set forth in this Office action:

13   *A patent may not be obtained though the invention is not identically*
14   *disclosed or described as set forth in section 102 of this title, if the differences*
15   *between the subject matter sought to be patented and the prior art are such that*
16   *the subject matter as a whole would have been obvious at the time the invention*
17   *was made to a person having ordinary skill in the art to which said subject matter*
18   *pertains. Patentability shall not be negatived by the manner in which the*
19   *invention was made.*
20

21   Claims 1, 3, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over

22   Hirotani (US Patent Number 5,982,887), further in view of Oishi (US Patent Number 6,907,125),

23   and further in view of Schneier (Applied Cryptography).

24   Regarding claim 1, Hirotani disclosed a control program for controlling an operation of a

25   microprocessor (See Hirotani Col. 4 Paragraph 3), the control program comprising a concealed

26   program (See Hirotani Col. 3 Paragraph 7), recoverable by data scramble circuit (See Hirotani

1   Col. 3 Paragraph 8) and a non-concealed program (See Hirotani Fig. 1 Element 15 wherein only

2   part of the program is encrypted). However, Hirotani failed to disclose the data scramble circuit

3   being a hardware circuit acting as part of an error correction circuit.

4   Oishi teaches that in order to protect against errors in a decryption system, error

5   correction can be combined with the decryption system by encrypting error correction codes as

6   well as the stored data and then decrypting the codes and using the codes in error correction (See

7   Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

8   Schneier teaches that encryption and decryption can be performed in a hardware circuit

9   (See Schneier Pages 223-225).

10   It would have been obvious to the ordinary person skilled in the art at the time of

11 invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by

12 utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and

13 further by providing a hardware decryption circuit to be used in place of the CPU decryption.

14 This would have been obvious because the ordinary person skilled in the art would have been

15 motivated to protect the integrity of the program in a cost efficient manner, and further would

16 have been motivated to increase the speed of the decryption, increase the security of the

17 decryption, ease in the installation of the decryption method, and increase the efficiency of the

18 CPU.

19   Regarding claim 3, the combination of Hirotani disclosed a device, comprising: a

20 microprocessor (See Hirotani Fig. 3 Element 21), a program memory for storing a control

21 program for controlling an operation of the microprocessor (See Hirotani Fig. 3 Element 25), the

22 control program including a concealed program (Element 25 Encrypted Section) and a non-

1   concealed program (Element 25 Program section); a rewritable memory for storing a copy of the

2   concealed program copied from the concealed program stored in the program memory (See

3   Hirotani Col. 6 Paragraph 2 and the rejection of claim 1 above wherein it was inherent that the

4   encrypted program was stored, at least temporarily in a rewritable memory in the decryption

5   circuit, before decryption), and a data scramble circuit for recovering the concealed program

6   stored in the rewritable memory as a recovered program (See Hirotani Col. 6 Paragraphs 2-3 and

7   the rejection of claim 1 above), but failed to disclose that the data scramble circuit was a

8   hardware circuit acting as part of an error correction circuit.

9   Oishi teaches that in order to protect against errors in a decryption system, error

10   correction can be combined with the decryption system by encrypting error correction codes as

11   well as the stored data and then decrypting the codes and using the codes in error correction (See

12   Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

13   Schneier teaches that encryption and decryption can be performed in a hardware circuit

14   (See Schneier Pages 223-225).

15   It would have been obvious to the ordinary person skilled in the art at the time of

16   invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by

17   utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and

18   further by providing a hardware decryption circuit to be used in place of the CPU decryption.

19   This would have been obvious because the ordinary person skilled in the art would have been

20   motivated to protect the integrity of the program in a cost efficient manner, and further would

21   have been motivated to increase the speed of the decryption, increase the security of the

1 decryption, ease in the installation of the decryption method, and increase the efficiency of the

2 CPU.

3   Regarding claim 6, the combination of Hirotani disclosed a method for creating a control

4 program, comprising: a program descramble step of descrambling a portion of a control program

5 by reverse scramble of a data scramble circuit in a device to be controlled, thereby creating a

6 concealed program as a portion of the control program (it was inherent in the invention of

7 Hirotani that a portion of the control program was encrypted in order for the control program to

8 have taken on the form of Element 25 in Fig. 3); and a program storing step of storing the control

9 program including the concealed program in a program memory so that the control program

10 controls an operation of a microprocessor in the device to be controlled (See Hirotani Col. 5 lines

11 39-44), but failed to disclose that the data scramble circuit was a hardware circuit acting as part

12 of an error correction circuit.

13   Oishi teaches that in order to protect against errors in a decryption system, error

14 correction can be combined with the decryption system by encrypting error correction codes as

15 well as the stored data and then decrypting the codes and using the codes in error correction (See

16 Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

17   Schneier teaches that encryption and decryption can be performed in a hardware circuit

18 (See Schneier Pages 223-225).

19   It would have been obvious to the ordinary person skilled in the art at the time of

20 invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by

21 utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and

22 further by providing a hardware decryption circuit to be used in place of the CPU decryption.

1   This would have been obvious because the ordinary person skilled in the art would have been

2   motivated to protect the integrity of the program in a cost efficient manner, and further would

3   have been motivated to increase the speed of the decryption, increase the security of the

4   decryption, ease in the installation of the decryption method, and increase the efficiency of the

5   CPU.

6   Regarding claim 8, the combination of Hirotani disclosed a method for operating a

7   control program, comprising: a program copying step of copying a concealed program which is a

8   portion of the control program (See Hirotani Fig. 3 Element 25) from a program memory into a

9   rewritable memory (See rejection of claim 3 above); a program recovery step of recovering the

10   concealed program copied by the program copying step as a recovered program by a data

11   scramble circuit (See rejection of claim 3 above); and a program execution step of executing a

12   non-concealed program included in the control program and the recovered program (See Hirotani

13   Col. 6 Paragraph 5), but failed to disclose that the data scramble circuit was a hardware circuit

14   acting as part of an error correction circuit.

15   Oishi teaches that in order to protect against errors in a decryption system, error

16   correction can be combined with the decryption system by encrypting error correction codes as

17   well as the stored data and then decrypting the codes and using the codes in error correction (See

18   Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

19   Schneier teaches that encryption and decryption can be performed in a hardware circuit

20   (See Schneier Pages 223-225).

21   It would have been obvious to the ordinary person skilled in the art at the time of

22   invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by

1   utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and

2   further by providing a hardware decryption circuit to be used in place of the CPU decryption.

3   This would have been obvious because the ordinary person skilled in the art would have been

4   motivated to protect the integrity of the program in a cost efficient manner, and further would

5   have been motivated to increase the speed of the decryption, increase the security of the

6   decryption, ease in the installation of the decryption method, and increase the efficiency of the

7   CPU.

8   Regarding claim 7, the combination of Hirotani, Oishi, and Schneier disclosed that the

9   program descramble step includes the steps of: creating a non-concealed program (it was

10   inherent that the program was created at some point in order for the program to have been

11   encrypted and downloaded); and synthesizing the concealed program and the non-concealed

12   program into the control program (See Hirotani Fig. 3 Element 25 wherein the encrypted and

13   non-encrypted programs are together as the program stored in program memory).

14   Regarding claim 9, the combination of Hirotani, Oishi and Schneier disclosed a program

15   erasure step of erasing the recovered program from the rewritable memory (See Hirotani Col. 6

16   Paragraph 6).

17   Claims 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the

18   combination of Hirotani, Oishi, and Schneier disclosed as applied to claims 1 and 3 respectively

19   above, and further in view of Oualline ("Practical C++ Programming") and Ooi et al. (U.S.

20   Patent Number 5,226,129) hereinafter referred to as Ooi.

21   The combination of Hirotani, Oishi, and Schneier disclosed a recoverable encrypted

22   program to be run on a microprocessor (See rejection of claim 1 above) but Hirotani failed to

1   disclose the composition of the program as well as the addressing mode of the program.

2   However, Hirotani did disclose that the encrypted program could have been downloaded over a

3   network (See Hirotani Col. 3 Lines 27-29).

4   Oualline teaches that in order to conserve memory space, commonly used code can be

5   grouped into functions such that the code can be used repeatedly (See Oualline Page 133

6   Paragraph 1). Ooi teaches that in order to easily make a program portable, the program should

7   use relative addressing (See Ooi Col. 1 Lines 27-33).

8   It would have been obvious to the ordinary person skilled in the art at the time of

9   invention to employ the teachings of Oualline to create functions in the encrypted program of

10   Hirotani, Oishi, and Schneier. This would have been obvious because the ordinary person

11   skilled in the art would have been motivated to make the program as compact as possible in

12   order to conserve memory and also to limit the amount of information needing to be transferred

13   over the network to the system of Hirotani. It further would have been obvious to the ordinary

14   person skilled in the art at the time of invention to employ the teachings of Ooi in the program of

15   Hirotani, Oishi, and Schneier by providing the program with relative addressing. This would

16   have been obvious because the ordinary person skilled in the art would have been motivated to

17   minimize the modification of the code required to relocate the program, and thus increase

18   portability.

19   It would have been obvious in the combination of Hirotani, Oishi, Schneier, Oualline,

20   and Ooi that relative address lists for the functions of the program would be provided in the

21   program at prescribed, or predetermined, location, in order for the processor of Hirotani to be

22   able to locate the functions called throughout the program.

1   *Conclusion*

2   Claims 1-3, and 5-9 have been rejected.

3   Any inquiry concerning this communication or earlier communications from the

4   examiner should be directed to Matthew T. Henning whose telephone number is (571) 272-3790.

5   The examiner can normally be reached on M-F 8-4.

6   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

7   supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the

8   organization where this application or proceeding is assigned is 571-273-8300.

9   Information regarding the status of an application may be obtained from the Patent

10 Application Information Retrieval (PAIR) system. Status information for published applications

11 may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

12 applications is available through Private PAIR only. For more information about the PAIR

13 system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

14 system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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17

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19   TECHNOLOGY CENTER 2100

20 Matthew Henning
21 Assistant Examiner
22 Art Unit 2131
23 9/9/2005